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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,094	HAIKONEN, PENTTI	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15 and 16* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed 12-7-2005.

Claim Objections

Claim 8 is objected to because of the following informalities:

"external input" on line 2 of claim appears to be --the external input--;

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Choy et al. (US PAT No. 5,789,944).

Regarding claim 1, Fig. 2 of Choy et al. teaches a circuit element comprising; one or more logically entangled bi-directional terminals (output terminals of 32 and 34), wherein each bi-directional terminal can assume any one of three logical states (32 controlled by 48 and 34 controlled by 50; col. 6, line 56 - col. 7, line 8), which are: (a) a logical true state (logic high; when driver 210 or 214 is enabled, 52 is driven either high or low based on respective input signal) (b) a logical false state (logic low; when driver 210 or 214 is enabled, 52 is driven either high or low based on respective input signal) and (c) an indefinite state (when control signals 48 or 50 disables the drivers 210 or 214, i.e. in high impedance state) in which state the bi-directional terminal accepts one

of the logical true and logical false states as an external input from an external source (setting 32 and 34 into a high impedance state is determined by the external input 36 from the external source 24) and an entanglement logic (26 is anticontention circuitry providing no contention on bus 52) for resolving the logical state of each of the bi-directional terminals according to a predetermined set of logical entanglement rules (based on the signal received on 36, 26 enables or disables input/output circuitry 32 and 34) between the bi-directional terminals.

Regarding claim 2, Fig. 2 of Choy et al. teaches a circuit element according to claim 1 where the entanglement logic is operable to perform the resolving in response to the external input from the external source (setting 32 and 34 into a high impedance state is determined by the external input 36 from the external source 24).

Regarding claim 3, Fig. 2 of Choy et al. teaches a circuit element according to claim 1, wherein the circuit element comprises several sets of logical entanglement rules (In Fig. 9 based on the data from 924, anticontention circuitry 928 resolve the contention on bus 972; col. 14, lines 23-60) and a set of additional terminals (terminals coupled to 36; two terminals receiving signals from 924 as shown in Fig. 9), each additional terminal accepting a logical true state or logical false state as an input (two terminal receives logic high or logic low), wherein the inputs to the set of additional terminals collectively determine which of several sets of logical entanglement rules are

to be used for said resolving (based on the data from 924, anticontention circuitry 928 resolve the contention on bus 972; col. 14, lines 23-60).

Regarding claim 4, Fig. 2 of Choy et al. teaches a circuit element according to claim 1, wherein the inputs to the set of additional terminals collectively determine the logical state of one or more of the bi-directional terminals (output of 210 which is an input to its output terminal 52 determines the state of receiver 216 terminal, and output of 214 which is an input to its output terminal 52 determines the state of receiver 212 terminal).

Regarding claim 5, Fig. 2 of Choy et al. teaches a circuit element according to claim 1, further comprising one or more circuit components, each of which has a high-impedance state, for implementing the indefinite state (tri-state drivers 210 and 214 provides an high impedance state).

Regarding claim 6, Fig. 2 of Choy et al. teaches a network for logical deduction, the network comprising: two or more circuit elements (32 and 34), each of which comprises: two or more logically entangled bi-directional terminals (output terminals of 32 and 34), wherein each bi-directional terminal can assume any one of three logical states, which are: (a) a logical true state (logic high; when driver 210 or 214 is enabled, 52 is driven either high or low based on respective input signal) (b) a logical false state (logic zero) and (c) an indefinite state (when control signals 48 or 50 disables the drivers

210 or 214, i.e. in high impedance state, the receiver 212 or 216 receives or accepts logic high or logic low which is driven externally to 32 from the 218 or 222), in which state the bi-directional terminal accepts one of the logical true and logical false states as an external input from an external source (210 and 214 receives external signal at node 218 and 222 respectively from the source external to 32 and 34) and an entanglement logic (30 in Fig. 4 resolves conflicts from the three-state select signals by providing an enable signal; col. 2, lines 46-54) for resolving the logical state of each of the bi-directional terminals according to a predetermined set of logical entanglement rules between the bi-directional terminals (based on the signal received on 36, 26 enables or disables input/output circuitry 32 and 34); wherein the network further comprises a set of additional terminals (terminals coupled to 36; two terminals receiving signals from 924 as shown in Fig. 9) wherein the inputs to the set of additional terminals collectively determine which of several sets of logical entanglement rules are to be used for the resolving (based on the data from 924, anticontention circuitry 928 resolve the contention on bus 972; col. 14, lines 23-60).

Regarding claim 7, Fig. 2 of Choy et al. teaches a network according to claim 6, further comprising an operational coupling (bus 52 connecting all bidirectional terminals of 32 and 34 in Fig. 2 and bus 972 in Fig. 9) of each of several bi-directional terminals of one or more logic elements to one or more additional terminals of another circuit terminal.

Regarding claim 8, Fig. 2 of Choy et al. teaches a network according to claim 7, where the operational coupling is modifiable by the external input (connection of all bidirectional terminals of 32 and 34 in Fig. 2 and bus 972 in Fig. 9 is modified by the data from 24 or 924).

Regarding claim 9, Fig. 2 of Choy et al. teaches a network according to claim 6, wherein each of several bi-directional terminals of one or more logic elements is operationally coupled to one or more bi-directional terminals of another circuit terminal (bus 972 couples 932, 934, 936 and 938).

Regarding claim 10, Fig. 2 of Choy et al. teaches a network according to claim 6, further comprising an interface to a data processing system for controlling and accessing some or all of the bi-directional terminals (driver select control circuitry 24 in Fig. 2 and 924 in Fig. 9 controls and accesses bidirectional terminals of 32 and 34 via the anticontention circuitry 26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choy et al. in view of Butts et al. (US PAT No. 5,734,581).

Regarding claims 15-16, Fig. 2 of Choy et al. teaches the circuit elements according to claims 1 and 6 as discussed above, but does not teach a computer program product including program instructions, wherein the program instructions cause a computer to simulate the circuit element. However, Butts et al. teaches hybrid simulation methods for the purpose of providing fast and detailed analysis of a logic circuit's operation. It would have been obvious at the time of invention to provide simulation of anticontention circuit of Choy et al. using the computer program and method of Butts et al. in order to analyze accurate timing interaction with the anticontention circuit.

Allowable Subject Matter

Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims as well as including all corrections to the claim objections stated above.

The following is a statement of reasons for the indication of allowable subject matter: one of ordinary skill in the art would not have been motivated to modify the teaching of Choy et al. et al. and/or Butts et al. to further includes, among other things, the specifics of bias elements for biasing one or more of the terminals of the network toward one of the logic states where each bias element is weak enough to be overridden by one of the circuit elements (claim 11).

Response to Arguments

Applicant's arguments with respect to claims 1-10 and 15-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Cho
Primary Examiner
Art Unit 2819

3-6-2006